REMARKS

Claims 1 – 8, 12 and 14 – 34 are pending in the present application, of which claims 15 – 34 have been withdrawn from consideration. By this Amendment, claim 2 has been amended. No new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated March 24, 2005.

Allowable Subject Matter:

Applicant gratefully acknowledges the indication that claims 1, 4, 12 and 14 have been allowed.

1. 35 U.S.C. §112 First Paragraph Rejection:

Claims 2, 3 and 5 – 8 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with it is most nearly connected, to make and/or use the invention.

This rejection is respectfully traversed.

From claim 2, as amended, it has become clear that the sidewall insulation film is formed covering the sidewalls of the first insulation film, the conductor pattern and the etching stopper film in the contact hole. Thus, withdrawal of the rejection of claims 2, 3 and 5-8 under 35 U.S.C. §112 is respectfully requested.

2. Claim Resection Under 35 U.S.C. §103:

(1) Claims 2, 3, 5, and 6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fukase (U.S.P. 5,728,595) in view of Kimura (U.S.P. 6,127,734). Claims 7 and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fukase in view of Kimura, and further in view of Hosotani et al. (U.S.P. 5,977,583).

Each of these rejections are respectfully traversed.

(2) Claim 2 has a feature that the first insulation film is filled in spaces between the adjacent conductor patterns and is not extending over the etching stopper film. According to this feature of the present invention, the contact hole can be formed in self-alignment with the conductor patterns. When the first insulation film is not extending over the etching stopper film, the end of the contact hole is defined by the conductor pattern. Thus, the contact holes, which are adjacent to each other with the conductor pattern interposed therebetween, can be formed by the mask pattern having one opening and formed in self-alignment with the conductor patterns. Thus, according to the present invention, pattern size of the mask pattern and the alignment allowance for forming the contact holes can be greatly increased, whereby the fabrication process can be simple and the fabrication cost can be lowered.

In Fukase, the interlayer insulating film 13 is formed over the etching stopper layer 7. The end of the contact hole 15 is defined by the side wall of the interlayer insulating film 13 (see, e.g., FIG. 2E). In Kimura, interlayer insulating layer 11 is formed over the gate electrode 7. The end of the contact hole 27 is defined by the side wall of the interlayer insulating layer 11

(see, e.g., FIG. 11). Thus, the semiconductor devices of Fukase and Kimura clearly differ from that of the present invention.

As described above, Fukase and Kimura clearly differ from the present invention and do not provide any motivation for the claimed invention. Thus, the present invention would have been unobvious to one of ordinary skill in the art at the time the invention was made, even if Fukase and Kimura are combined.

(3) The Examiner states that in the configuration of an interlayer insulating film formed on gates without sidewall spacers, the device can be manufactured with a lower number of steps and higher degree of integration (Kimura, col. 5, lines 50-56).

However, in Kimura, in order to form the contact hole having smaller opening diameter in the interlayer insulating layer 11, the sidewall insulation film 17 for patterning the insulating layer 13 is formed over the interlayer insulating layer 11. Thus, in Kimura, whether or not the sidewall insulation film is formed on the side wall of the gate electrode 7, the diameter of the contact hole is defined by the sidewall insulation film 17. The presence or absence of the sidewall insulation film formed on the side walls of the gate electrodes 7 has no relation with the semiconductor device of Kimura. Thus, Kimura has no relation with the present invention.

(4) In Hosotani et al., the first BPSG film 22 is filled in spaces between the adjacent gate electrodes 19 and is not extending over the first silicon nitride film 17 (see, e.g., FIG. 13). However, in Hosotani et al., the sidewalls 21 are formed on the side walls of the gate electrodes

19. The sidewall 21 is formed between the gate electrode 19 and the first BPSG film 22 (see, e.g., FIG. 11). The sidewall 21 is not formed on the first BPSG film 22 in the contact hole (see, e.g., FIG. 12). Thus, the semiconductor device of Hosotani et al. clearly differs from that of the present invention.

In Hosotani et al, the first BPSG film 22 and the contact hole are formed after the formation of the sidewall 21. The contact hole is formed in the first BPSG film 22 with the sidewall 21 as the etching stopper. Thus, sidewall 21 must be formed of the material having etching characteristics different from those of the first BPSG film. In the silicon-based semiconductor device, the silicon oxide-based materials are often used as the interlayer insulating film, and the silicon nitride-based material is often used as the etching stopper film. Also in Hosotani et al, the sidewall 21 is formed of the silicon nitride film. (see, e.g., column 8, lines 31-34). However, when the sidewall 21 of the silicon nitride film is formed between the gate electrode 19 and the first BPSG film 22, the dielectric constant of the interlayer insulating film is increased and which causes the degradation of the high-speed performance, because of high dielectric constant of the silicon nitride.

In claim 2, the sidewall insulation film is formed covering the side walls of the first insulation film, the conductor pattern and the etching stopper film in the contact hole. The first insulation film is formed in contact with the sidewalls of the conductor patterns. These features mean that the sidewall insulation film is formed after the formation of the first insulation film and the contact hole. According to this, the sidewall insulation film is unnecessary for using the etching stopper. Thus, the sidewall insulation film can be formed of the silicon oxide-based material having low

dielectric constant, whereby the dielectric constant of the interlayer insulation film can be lowered. The sidewall insulation film does not undergo the etching damage, whereby the dielectric breakdown voltage of the interlayer insulation film can be improved. Thus, claim 2 clearly differs from Hosotani et al.

Thus, the present invention would have been unobvious to one of ordinary skill in the art at the time the invention was made, even if Fukase, Kimura, and Hosotani et al. are combined.

In view of the aforementioned amendments and accompanying remarks, Applicant submits that that the claims, as herein amended, are in condition for allowance. Applicant requests such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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